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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,055	03/23/2001	Yuji Takaoka	09792909-4794	5918

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EXAMINER	
BEREZNY, NEMA O	
ART UNIT	PAPER NUMBER
2813	11

DATE MAILED: 11/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/816,055	Applicant(s) TAKAOKA	
	Examiner Nema O Berezny	Art Unit 2813	

-- Th MAILING DATE of this communication app ars on the cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *17-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *04 September 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The objection to drawings, made in prior Office Action mailed 7-12-02 is hereby withdrawn, subsequent to corrections made by Applicant in Amendment A, filed 9-4-02.

Specification

The objections to specification, made in prior Office Action mailed 7-12-02 are hereby withdrawn, subsequent to corrections made by Applicant in Amendment A, filed 9-4-02.

Claim Objections

The objections to claims 1 and 7, made in prior Office Action mailed 7-12-02 are hereby withdrawn, subsequent to corrections made by Applicant in Amendment A, filed 9-4-02.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Fjelstad (6,284,563). Fjelstad discloses a semiconductor device, comprising: a plurality of semiconductor chips (Fig.15 el.900; col.5 lines 55-65) mounted on an outer surface of a substrate (no #); an insulation film (el.940) provided on said substrate, wherein a top surface and side surfaces of said chips are encrusted in said insulation film (Fig.15); wiring (el.970) provided on said insulation film, wherein said wiring is connected to said chips through a connection hole (el.955) formed on said insulation film; an upper layer insulation film (el.980) provided on said insulation film that covers said wiring; and an electrode (col.6 lines 28-37) provided on said upper layer insulation film that is connected to said wiring through a connection hole (el.983) formed on said upper layer insulation film. Fjelstad also discloses wiring that is arranged such that a shared circuit exists between two chips of said plurality of chips (col.8 lines 13-19), wherein said shared circuit is an input-output interface for an external equipment (col.6 lines 28-37).

Claims 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Eichelberger (6,159,767). Eichelberger discloses a semiconductor device, comprising: an insulation layer (Fig.5g el.106,104) supporting a plurality of semiconductor chips (el.102), wherein a top surface and at least a portion of side surfaces of said chips are encrusted in said insulation layer, and a surface opposite said top surface of said chips is exposed (Fig.5g); wiring (no #) provided on said insulation layer that is connected to

each chip through a connection hole formed on said insulation layer (Fig.5g); an upper layer insulation film (el.150) provided on said insulation layer that covers said wiring; and an electrode (el.154) provided on said upper layer insulation film that is connected to said wiring through a connection hole formed on said upper layer insulation film. Eichelberger also discloses wiring that is arranged such that a shared circuit exists between two chips of said plurality of chips (col.8 lines 66-67), and a shared circuit that is an input-output interface circuit for an external equipment (el.152).

Claims 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Fillion et al. (6,239,980). Fillion discloses a semiconductor device, comprising: a plurality of chips (Fig.1 el.22,24) mounted on a substrate (el.38; col.5 lines 51-56); an insulation film (el.53) on said substrate, wherein said plurality of chips is encrusted in said insulation film (Fig.1); wiring (el.74) provided on said insulation film and connected to said chips through a connection hole in said insulation film, wherein said wiring is a shared circuit between two or more of said plurality of chips (Fig.1); and an external electrode (el.212) provided on said upper insulation film, connected to said wiring through a connection hole (el.210) formed on said upper insulation film (col.8 lines 49-53).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fjelstad as applied to claims 1-4 above, and further in view of Sharma (5,552,633). Fjelstad does not disclose a shared power supply circuit or a shared electrostatic protection circuit. However, Sharma discloses a multi-chip module in which shared circuitry for power and electrostatic protection is provided (col.8 lines 3-21). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the shared power and electrostatic protection circuitry of Sharma with the semiconductor device of Fjelstad in order to couple power to a chip through a low ohmic resistance path (Sharma – col.8 lines 7-13), and to provide electrostatic discharge protection to the integrated device through the ground terminal (col.8 lines 13-21).

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fillion as applied to claims 13-14 above, and further in view of Sharma (5,552,633). Fillion does not disclose a shared power supply circuit or a shared electrostatic protection circuit. However, Sharma discloses a multi-chip module in which shared circuitry for power and electrostatic protection is provided (col.8 lines 3-21). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the shared power and electrostatic protection circuitry of Sharma with the semiconductor device of Fillion in order to couple power to a chip through a low ohmic

resistance path (Sharma – col.8 lines 7-13), and to provide electrostatic discharge protection to the integrated device through the ground terminal (col.8 lines 13-21).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger as applied to claims 7-10 above, and further in view of Sudo (5,475,264). Eichelberger does not disclose a shared power supply circuit. Sudo discloses a shared power supply circuit (col.3 lines 35-46) for a multi-chip module. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the shared power supply circuit of Sudo with the semiconductor device of Eichelberger in order to supply adequate power to either chip when needed, without requiring both chips to be high power chips.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger as applied to claims 7-10 above, and further in view of Sharma (5,552,633). Eichelberger does not disclose a shared electrostatic protection circuit. However, Sharma discloses a multi-chip module in which shared circuitry for electrostatic protection is provided (col.8 lines 17-21). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the shared electrostatic protection circuitry of Sharma with the semiconductor device of Eichelberger in order to provide electrostatic discharge protection to the integrated device through the ground terminal (col.8 lines 13-21).

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 9-4-02 with respect to claims 13-16 have been fully considered but they are not persuasive. Applicant contends that Fillion does not disclose a shared circuit between two chips. However, Applicant also pointed out that a metallization (74) exists between the two chips (22,24), which constitutes a shared circuit between the two chips. An interconnection (i.e. the metallization 74) is defined as "a transmission line connecting two electric systems or networks and permitting energy to be transferred in either direction" ("Modern Dictionary of Electronics," p.507), hence a shared circuit.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (703) 305-3445. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NB
October 23, 2002

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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